

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on November 2, 2006, and the references cited therewith.

Claims 1, 3, 4, 5, 6 and 8 have been amended. Claims 14-20 (of which claims 15-20 were subject to a Restriction Requirement) are canceled, and Applicant reserves the right to pursue these claims in this or continuing applications. In response to paragraph 1 of the Office Action, the claims are presented to correct minor informalities to reflect the Examiner's amendment in the Notice Of Allowance mailed September 15, 2005. Claim 6 has been amended to address the informality noted in paragraph 4 of the Office Action. As a result, claims 1-13 are now pending in this application. Also, Applicant respectfully submits that a substitute Declaration will be submitted upon allowance of the application. Finally, Applicant thanks the Examiner for the courtesies extended during the interview of April 17, 2007. Applicant believes that the present response reflects the substance of that interview.

'103 Rejection of the Claims

Claims 1-13 were rejected under 35 USC ' 103(a) as being unpatentable over *Maupin* (U.S. Patent 6,154,832). Applicant disagrees with these rejections because *Maupin* does not teach or suggest the subject matter of at least independent claims 1 or 8, as amended. Applicant requests withdrawal of the rejections and allowance of the claims.

Claim 1 as amended recites in pertinent part and with emphasis added:

A method of performing a context switch operation, comprising:

setting an index register on an address portion of a state machine in a peripheral system to a first index value by a host computer, the first index value indicating a first register to be accessed;

accessing context data in the first register of the peripheral system based upon the first index value;

setting the index register to a **second index value by a the host computer**, the second index value indicating a second register to be accessed;

accessing context data in the second register of the peripheral system when the index register is set to the second index value, **wherein the first and second registers are collocated with the peripheral system.**

Respectfully, *Maupin* does not teach or suggest a host computer setting an index register on an address portion of a state machine in a peripheral system to a first and second value as

recited in claim 1. The Office Action contends that the registers are collocated with the peripheral system inasmuch as the embedded controller 10 of Maupin is considered to be the peripheral system and the host computer is considered to be external to the embedded controller 10 of Maupin (see, e.g., paragraphs 8 and 16 of the Office Action).

However, Maupin does not show setting an index value in an address portion of state machine on the embedded controller, as would be required if the embedded controller in Maupin were a peripheral system. Moreover, Maupin does not show that a “host computer” (under the present interpretation of the Office Action, as referenced above) sets a first and second index value in the embedded controller. That is, as the Office Action contends that the host computer is external to the embedded controller, there is no showing in Maupin that the host computer causes a first index value and a second index value to be set on the embedded controller.

Claim 1 further recites a state machine in the peripheral system. The Office Action argues with respect to claim 10, that *Maupin* discloses a state machine. However, under the Examiner’s interpretation the embedded controller is a peripheral system and the embedded controller does not contain a state machine, as recited in claim 1. Therefore, *Maupin* does not teach or suggest a state machine in a peripheral system, as required by claim 1.

Alternatively, even if the register file 44 of Maupin is considered a peripheral system to the execution core 40 of Maupin, the execution core 40 does not provide any index values to the register file 44. Nor does the register file 44 include a state machine.

Thus, *Maupin* does not teach or suggest a host computer setting an index register on an address portion of a state machine in a peripheral system. Nor does *Maupin* teach or suggest a host computer setting an index register to first index value and a second index value. For at least these reasons, claim 1 is allowable because *Maupin* does not disclose all the elements of claim 1.

Claims 2-7 depend from claim 1 and are allowable for the reasons claim 1 is allowable. Claim 8 includes limitations similar to claim 1. Thus, for at least the reasons stated above with respect to claim 1, claim 8 is allowable. Claims 9-13 depend from claim 8 and are allowable for at least the reasons claim 8 is allowable.

Double Patenting Rejection of the Claims

Claims 1-13 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4-5 of copending application No. 11/314,036 in view of *Maupin*.

Respectfully, a terminal disclaimer will be filed in the later-allowed of the 11/314,036 application and the present application.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (202-470-6452) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-3521.

Respectfully submitted,
Brake Hughes Bellermann LLP
Customer Number 57246
202-470-6452



April 25, 2007
Date

William G. Hughes
Reg. No. 46,112